ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS
(MR13 Regulations)

For

M.Tech. (DIGITAL SYSTEMS & COMPUTER ELECTRONICS)

(Applicable for the batches admitted from academic year 2013-14)

Department of Electrical & Electronics Engineering
MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

Maisammaguda, Dulapally (post & via Kompally), Secunderabsd-500 100

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MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

Maisammaguda, Dhulapally (Post via. Kompally), Secunderabad – 500100

ACADEMIC REGULATIONS MR 13 FOR M. TECH. (REGULAR) DEGREE COURSE

(Effective for the students admitted into first year from the academic year 2013-2014)

The M.Tech Degree of Malla Reddy Engineering College, Hyderabad shall be conferred on candidates by the Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to the eligibility, qualifications and Specialization as prescribed by the university/college from time to time.

Admissions shall be made on the basis of merit/rank obtained by the qualifying candidate at an Entrance Test conducted by the University/college or on the basis of any other order of merit approved by the University/college (say **PGECET/GATE)** subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four Academic years from the year of his admission, shall forfeit his seat in M. Tech. course.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The minimum instruction days in each semester are 90.

3.0 A. COURSES OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Advanced Manufacturing Systems(AMS) - Shift II
2. Computer Science(CS) - Shift I
3. Computer Science and Engineering(CSE) - Shift I & II
4. Control Engineering(CE) - Shift I
5. Control Systems(CS) - Shift I & II
6. Digital Systems and Computer Electronics(DSCE) - Shift I & II
7. Embedded Systems(ES) - Shift I
8. Geotechnical Engineering(GTE) - Shift I
9. Power Electronics and Electrical Drives(PEED) - Shift II
10. Structural Engineering(SE) - Shift I
11. Transportation Engineering(TE) - Shift II
12. Thermal Engineering(THE) - Shift I
13. VLSI System Design(VLSI SD) - Shift I

3.0 B. Departments offering M. Tech. Programmes with specializations are noted below:

Civil Engineering Department.	1. Structural Engineering(SE) 2. Transportation Engineering(TE) 3. Geotechnical Engineering(GTE)
Computer Science & Engineering Department	1. Computer Science(CS) 2. Computer Science and Engineering(CSE)
Electrical & Electronics Engineering Department	1. Control Systems(CS) 2. Control Engineering(CE) 3. Power Electronics and Electrical Drives(PEED)
Electronics & Communication Engineering Department	1.Digital Systems and Computer Electronics(DSCE) 2. VLSI System Design(VLSI SD) 3. Embedded Systems(ES)
Mechanical Engineering Department	1. Thermal Engineering(THE) 2. Advanced Manufacturing Systems(AMS)

4.0 ATTENDANCE

The programs are offered on a unit basis with each subject being considered a unit.

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

4.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the previous semester including the days of attendance in sports, games, NCC and NSS activities.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 75 marks shall be awarded based on the performance in the End Semester Examination and 25 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with Part A as one question to be answered out of two questions, which carries 10 marks and Part B with 3 questions to be answered out of 5 questions each question for 5 marks. If any candidate is absent for any subject of a mid -term examination, an additional exam will be conducted in the deserving cases based on the recommendations of the College Academic Committee. End semester examination is conducted for 75 marks with 5 questions to be answered out of 8 questions, each question carries 15 marks.

5.2 For practical subjects, 75 marks shall be awarded based on the performance in the End Semester Examinations and 25 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.5) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation after taking up a topic approved by the Project Review Committee(PRC).

6.1 A Project Review Committee shall be constituted with Principal as chair person, Head of the Department, Coordinator, Supervisor and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for its approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the Project work. Departmental Committee(DAC) Consists of Head of the Department as Chairman, along with two Senior Professors and few subject experts too.

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of topic as the case may be.

6.5 Candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation/demonstration before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/ Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the College. For this, Head of the Department shall submit a panel of 3 examiners to the Chief Controller of Examinations of the College, who are eminent in that field with the help of the concerned guide and Head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, he will not be eligible for the award of the degree unless he is asked to revise and resubmit by the Board.

7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70 but not less than 60%
Second Class	Below 60% but not less than 50%
Pass Class	Below 50% but not less than 40%

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8.0 WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the university or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS

9.1 Discontinued, detained or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.
9.2 The candidate who fails in any subject will be given two chances to pass the same subject:otherwise, he has to identify an equivalent subject as per MR13 academic regulations.

10.0 GENERAL

10.1 The academic regulations should be read as a whole for purpose of any interpretation.
10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.
10.3 The College may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the College.
10.4 Wherever the word he, him or his occur, it will also include she, her and hers.
10.5 Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject' and 'Practical Subject' or 'Lab'.
10.5 Transfers not allowed among group colleges.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any mark son the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shallot be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject tithe academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject

6	Refuses to obey the orders of the Chief Superintendent/Assistant –Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to the person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-incharge,or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police cases registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.

12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action toward suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

M.Tech (DIGITAL SYSTEM AND COMPUTER ELECTRONICS)

COURSE STRUCTURE AND SYLLABUS

2013-2014

I Year- I Semester

Code	Group	Subject	L	T	P	Credits
MR134101	Core	VLSI technology & design	3	1	0	3
MR134102	Core	Digital system design	3	1	0	3
MR134103	Core	Advanced data communications	3	1	0	3
MR134104	Core	Micro controllers for embedded system design	3	1	0	3
 MR134105 MR134106 MR134107	Elective I:	 Coding Theory and Techniques Image & video processing Embedded system design	3	1	0	3
 MR134108 MR135128 MR135129	Elective II	 CMOS digital integrated circuit design Internetworking Soft Computing Techniques	3	1	0	3
MR134109	Lab	Simulation lab	0	0	2	2
MR134110		Seminar	-	-	-	2
		Total Credits				22

Year - II Semester

Code	Group	Subject	L	T	P	Credits
MR135130	Core	Advanced computer architecture	3	1	0	3
MR134111	Core	Low power VLSI design	3	1	0	3
MR134112	Core	Design for testability	3	1	0	3
MR134113	Core	Embedded real time operating systems	3	1	0	3
MR134114 MR135131 MR134115	Elective III	CPLD & FPGA architectures and applications Network security & cryptography System on chip architecture	3	1	0	3
MR134116 MR134117 MR134118	Elective IV	CMOS mixed signal circuit design Digital signal processors and architectures Design fault tolerant systems	3	1	0	3
MR134119	Lab	Embedded system design lab	0	0	2	2
MR134120		Seminar	-	-	-	2
		Total Credits				22

II Year –I & II Semester

Code	Subject	L	P	Credits
MR134121	Comprehensive Viva	-	-	4
MR134122	Project work and Seminar	-	-	40
	Total			44

MALLAREDDY ENGINEERING COLLEGE
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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

VLSI TECHNOLOGY AND DESIGN

UNIT I Review Of Microelectronics And Introduction To Mos Technologies:
MOS, CMOS, BiCMOS Technology.Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT II Layout Design And Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
LOGIC GATES & LAYOUTS:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT III Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT IV Sequential Systems
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT V Floor Planning
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005,PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

DIGITAL SYSTEM DESIGN

UNIT I Minimization And Transformation Of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT II Digital Design:
Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT III Sm Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT IV Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT V Fault Diagnosis In Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH

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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

ADVANCED DATA COMMUNICATIONS

UNIT I Digital Modulation Schemes:
BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT II Basic Concepts Of Data Communications, Interfaces And Modems:
Data Communication Networks, Protocols and Standards, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/IP Protocol suite and Comparison with OSI model.

UNIT III Error Correction:
Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code
Data Link Control: Line Discipline, Flow Control, Error Control
Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.

UNIT IV Multiplexing:
Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL.
Local Area Networks: Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.
Metropolitan Area Networks: IEEE 802.6, SMDS
Switching: Circuit Switching, Packet Switching, Message Switching.
Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.

UNIT V Multiple Access Techniques:
Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access withCollision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing,
Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:
1. Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI.

REFERENCE BOOKS:
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th Ed., 2007, PHI.
3. Data Communication and Tele Processing Systems -T. Housely, 2nd Ed, 2008, BSP.
4. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2005,

MALLAREDDY ENGINEERING COLLEGE
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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT I Arm Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT II Arm Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT III Arm Programming Model – Ii:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT IV Arm Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT V Memory Management:
Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:
1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N.Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:
1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes/ Cole, 1999, Thomas Learning.

MALLAREDDY ENGINEERING COLLEGE
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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

CODING THEORY AND TECHNIQUES
(ELECTIVE -I)

UNIT I:
Source coding: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes,Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

UNIT II:
Linear Block codes: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes. Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

UNIT III:
Cyclic Codes: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

UNIT IV:
Convolutional Codes: encoding of Convolutional codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

UNIT V:
BCH Codes: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS :
1. Error Control Coding – Fundamentals and Applications by SHU LIN and Daniel J. Costello, Jr. Prentice Hall Inc.
2. Digital Communications – Fundamental and Application by Bernard sklar, Pearson Education Asia.
3. Error Control Coding Theory by Man Young Rhee, Mc. Graw Hill Publ.

REFERENCE BOOKS :
1. Digital Communications – John G. Proakis, Mc. Graw Hill Publication.
2. Digital and Analog Communication Systems – K. Sam Shanmugam
3. Digital Communications by Symon Haykin.

MALLAREDDY ENGINEERING COLLEGE
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M. Tech (DSCE)	L	T/P/D	C
I Year I Semester	3	1 /-/-	3

IMAGE AND VIDEO PROCESSING
(ELECTIVE -I)

UNIT I Fundamentals of Image Processing and Image Transforms:
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.
Image Segmentation:
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT II Image Enhancement:
Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT III Image Compression:
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy,
Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT IV Basic Steps of Video Processing:
Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT V 2-D Motion Estimation:
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:
1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang.1st Ed., PH Int.

REFRENCE BOOKS:
1. Digital Image Processing and Analysis-Human and Computer Vision Application with CVIP Tools – Scotte Umbaugh, 2nd Ed, CRC Press, 2011.
2. Digital Video Processing – M. Tekalp, Prentice Hall International.
3. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009.
4. Multidimentional Signal, Image and Video Processing and Coding – John Woods, 2nd Ed,Elsevier.
5. Digital Image Processing with MATLAB and Labview – Vipula Singh, Elsevier.
6. Video Demystified – A Hand Book for the Digital Engineer – Keith Jack, 5th Ed., Elsevier.

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EMBEDDED SYSTEM DESIGN
(ELECTIVE -I)

UNIT I Introduction to Embedded Systems:
Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT II Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(ELECTIVE - II)

UNIT I MOS Design
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT II Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT IV Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS
1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI

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INTERNETWORKING
(ELECTIVE - II)

UNIT I Internetworking Concepts:
Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of the Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address
Classful Addressing
Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting
Classless Addressing:
Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.
ARP and RARP: ARP, ARP Package, RARP.

UNIT II Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.
Transmission Control Protocol (TCP):
TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.
Stream Control Transmission Protocol (SCTP):
SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.
Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.
Classical TCP Improvements:
Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

UNIT III Unicast Routing Protocols (RIP, OSPF, and BGP):
Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.
Multicasting and Multicast Routing Protocols:
Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT IV
Domain Name System (DNS):Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet. Remote Login TELNET: Concept, Network Virtual Terminal (NVT).
File Transfer FTP and TFTP: File Transfer Protocol (FTP). Electronic Mail: SMTP and POP.
Network Management-SNMP: Concept, Management Components, World Wide Web- HTTP Architecture.

UNIT V Multimedia:
Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:
1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3rd Edition PHI

REFERENCE BOOKS:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.
5. The Internet and Its Protocols – Adrin Farrel, Elsevier, 2005.

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SOFT COMPUTING TECHNIQUES
(ELECTIVE -II)

UNIT I Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rulebased systems, the AI approach, Knowledge representation - Expert systems.

UNIT II Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT III Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning,
Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Selforganizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT IV Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters,
Solution of typical control problems using genetic algorithm, Concept on some other search
techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT V Applications:
GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:
1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:
1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt.Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.

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SIMULATION LAB

Note:A. Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted. Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.
1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II: VLSI Back End Design programs:
Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design/Transistorlevel design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).
1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
Basic logic gates
CMOS inverter
CMOS NOR/ NAND gates
CMOS XOR and MUX gates
CMOS 1-bit full adder
Static / Dynamic logic circuit (register cell)
Latch
Pass transistor
4.Layout of any combinational circuit (complex CMOS logic gate)- Learni

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ADVANCED COMPUTER ARCHITECTURE

UNIT I Fundamentals of Computer Design:
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressingtype and size of operands, Operations in the instruction set.

UNIT II Pipelines:
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design:
Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT III Instruction Level Parallelism (ILP) - The Hardware Approach:
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.
ILP Software Approach:
Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT IV Multi Processors and Thread Level Parallelism:
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain,Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT V Inter Connection and Networks:
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:
1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:
1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

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LOW POWER VLSI DESIGN

UNIT I Fundamentals:
Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II Low-Power Design Approaches:
Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III Low-Voltage Low-Power Adders:
Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V Low-Voltage Low-Power Memories:
Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan, Springer, 2005.

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DESIGN FOR TESTABILITY

UNIT I Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT II Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT III Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT IV Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT V Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT I Introduction:
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT II Real Time Operating Systems:
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT III Objects, Services and I/O:
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O
Concepts, I/O Subsystem

UNIT IV Exceptions, Interrupts and Timers:
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT V Case Studies of RTOS:
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS and Basic Concepts of Android OS.

TEXT BOOKS:
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS
(ELECTIVE -III)

UNIT I Introduction to Programmable Logic Devices:
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III SRAM Programmable FPGAs:
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2.Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE -III)

UNIT –I Introduction:
Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT –II Modern Techniques:
Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
Algorithms:
Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.
Conventional Encryption:
Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
Public Key Cryptography:
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT III Number Theory:
Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
Message authentication and Hash Functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT IV Hash and Mac Algorithms:
MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.
Digital signatures and Authentication Protocols:
Digital signatures, Authentication Protocols, Digital signature standards.
Authentication Applications:
Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT V IP Security:
Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.
Intruders, Viruses and Worms: Intruders, Viruses and Related threats.
Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)

2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

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SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -III)

UNIT I Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II Processors:
Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III Memory Design for SOC:
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV Interconnect Customization and Configuration:
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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CMOS MIXED SIGNAL CIRCUIT DESIGN
(ELECTIVE -IV)

UNIT I Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT V Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:
1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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I Year II Semester	3	1 /-/-	3

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -IV)

UNIT I Introduction to Digital Signal Processing:
Introduction, a Digital signal-processing system, the sampling process, discrete time sequences.
Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT III Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs,
Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX
Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV Analog Devices Family of DSP Devices:
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base
Architecture of ADSP 2100, ADSP-2181 high performance Processor.
Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal
Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT V Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:
1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran,
Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:
1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

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DESIGN OF FAULT TOLERANT SYSTEMS
(ELECTIVE -IV)

UNIT I Fault Tolerant Design

Basic Concepts: Reliability Concepts, Failure & Faults, Reliability and Failure rate, Relation between Reliability and Meantime between failure, Maintainability and Availability, Reliability of series, parallel and Parallel – Series combinational circuits.

Fault Tolerant Design: Basic Concepts – Static, dynamic, hybrid Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR Re-Configuration techniques, Use of error correcting code. Time redundancy and software redundancy

UNIT II Self Checking Circuits & Fail Safe Design

Self Checking circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, checkers using m out of n codes, Berger code, Low Cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA Design

UNIT III Atpg Fundamentals & Design For Testability For Combinational Circuit

Introduction to ATPG, ATPG Process – Testability and Fault analysis methods – Fault masking – Transition delay fault ATPG, Path delay, fault ATPG.

Design for Testability for Combinational Circuits : Basic concepts of Testability, Controllability and Observability, The Reed Muller's expansion technique, OR-AND-OR Design, Use of control and Syndrome Testable Designs

UNIT IV Scan Architectures & Techniques

Introduction to Scan Based testing, Functional testing, The Scan effective Circuit, The MUX-D Stule Scan flip-flops, The Scan shift register, scan cell operation

Scan test sequencing, scan testing timing, partial scan, multiple scan chains, scan based design rules (LSSD) At-speed scan testing and Architecture, multiple clock and scan domain operation, critical paths for At speed scan test.

UNIT V Built In Self Test (Bist)

BIST concepts, Tests Pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, Memory Test architecture.

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design – Parag K. Lala, 1984, PHI
2. Design for Test for Digital IC's and Embedded Core Systems – Alfred L. Crouch 2008, Pearson Education.

REFERENCE BOOKS:

1. Digital Systems Testing and testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing – Bushnell & Vishwani D.Agarwal, Springers.

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EMBEDDED SYSTEM DESIGN LAB

Note:
The following programs are to be implemented on ARM based Processors/Equivalent.
Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I:
The following Programs are to be implemented on ARM Processor
1. Simple Assembly Program for
a. Addition | Subtraction | Multiplication | Division
b. Operating Modes, System Calls and Interrupts
c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:
Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:
1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs (Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.